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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/970,929	10/05/2001	Jun Koyama	740756-2368	3139

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EXAMINER	
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ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/970,929	KOYAMA ET AL.	
	Examiner	Art Unit	
	Srilakshmi K. Kumar	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,37-54,73-90,109-126 and 145-184* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18, 37-54, 73-90, 109-126, 145-184* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The following office action is in response to the amendment filed on June 26, 2006. Claims 1-18, 37-54, 73-90, 109-126, 145-184 are pending. Claims 1, 10, 37, 46, 73, 82, 109, 118, 145, 152, 159, 166 are amended.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. ***Claims 1-9, 37-45, 145-151, 173, and 181,*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. (U.S. Patent No. 5,953,003) and Marshall et al. (U.S. Patent No. 6,121,760).

With reference to **claims 1, 37, and 145** Kwon et al. teaches a display device (60) comprising: a source signal line driving circuit (50) and a gate line driving circuit (40); a pixel portion (61-69); a shift register (42, 52) included in the source signal line driving circuit and in

the gate line driving circuit (see Figure 3) for outputting a pulse in accordance with clock signals (see column 4, lines 2-8); a level shifter (44, 56) included in the driving circuits for converting a voltage amplitude of input signals (see column 4, lines 17-20; 53-57); and a current source (46, 58) for supplying a current to the level shifter based on the pulse from the shift register(see column 4, lines 15-20; 46-57).

Kwon fails to specifically teach wherein only when said shift register serially outputs the pulses, said current source supplies the current and said level shifter is operated.

Marshall et al. teaches a power regulator wherein a shift register, having a plurality of stages, or units (see column 2, lines 9-15), operates with respect to clock pulses from a clock signal in which the clock signals are generated in association with the power control pulses. That is upon initiation of the power regulator a fist clock signal is output to the shift register, the shift register output terminals are set to a first level and the shift register will output a signal on successive occurrences of the second clocking signal (see column 5, line 16-column 6, line 15).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of the shift register with multiple stages wherein power is only provided when the shift register output pulses as taught by Marshall et al. in a device similar to that which is taught by Kwon et al. in order to thereby provide a display device in order to improve power regulation for reducing power consumption of the display.

With reference to **claims 2, 38, and 146**, while not specifically teaching that the source and gate line driving circuits and the pixel portion are provided over a glass substrate, Kwon et al. does teach conventional active matrix displays including a plurality of transistors and capacitors on a glass substrate (see column 1, lines 32-35).

The examiner takes Official Notice in that it is well known to one skilled in the art, for the source and gate line driving circuits and the pixel portion to be provided over a glass substrate.

Therefore it would have been obvious to one having ordinary skill in the art to allow for the source line driving circuit, the gate line driving circuit, and the pixel portion to be provided over a glass substrate as well known in the art and suggested by Kwon et al. in order to provide a transparent surface for constructing the display device for displaying images.

With reference to **claims 3, 4, 39, and 40**, neither Kwon et al. nor Marshall teaches that the driving circuit is provided on the same or different substrate as the pixel portion.

However, while not specifically teaching that the driving circuits and the pixels circuits are disposed on the same or different substrates, the Examiner takes Official notice in that conventional display devices are well known to have both of these configurations.

Therefore it would have been obvious to one having ordinary skill in the art to allow for the driving circuits and the pixels to be formed on the display substrates in accordance with what is conventionally known allowing placement on either one substrate or both of the substrates in order to produce a display device capable of display images.

With reference to **claims 5-9, 41-45, and 147-151**, while Kwon et al. teaches the usage of flat displays such as liquid crystal display (see column 1, lines 15-20) there fails to be any disclosure of the display device being incorporated into a personal computer, portable information terminal, car audio set, or digital camera.

However, the examiner takes Official Notice in that it is well known in the art for display device, preferably LCD device to be incorporated into personal computers, portable information terminals, car audio sets, and digital cameras.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of the LCD, similar to that which is taught by Kwon et al. in a wide range of user devices thereby providing the user with a clearer image of the displayed information.

With reference to **claims 173, 175, and 181**, while Kwon et al. teaches the usage of a source signal line driving circuit and a gate signal line driving circuit, wherein the source signal line driving circuit includes a latch type transmission array comprising thin film transistors (see column 5, line 45-column 6, line 12), there fails to be any other specific disclosure of the driving circuits comprising thin film transistors.

However, the examiner takes Official Notice in that it is well known in the art for the driving circuits of a display device to comprise of thin film transistors.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of thin film transistors in the driving circuits in order to thereby provide appropriate driving signals to drive the image onto the display device.

4. ***Claims 10-18, 46-54, 73-90, 109-126, 152-172, 174, 176-180, and 182-184*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. in view of Callahan et al. (U.S. Patent No. 5,574,475) and Marshall et al.

With reference to **claims 10, 46, 73, 82, 109, 118, 152, 159, and 166** Kwon et al. teaches a display device (60) comprising: a source signal line driving circuit (50) and a gate line driving circuit (40); a pixel portion (61-69); a shift register (42, 52) included in the source signal line driving circuit and in the gate line driving circuit (see Figure 3) for outputting a pulse in accordance with clock signals (see column 4, lines 2-8); a level shifter (44, 56) included in the driving circuits for converting a voltage amplitude of input signals (see column 4, lines 17-20; 53-57); and a current source (46, 58) provided in the source and gate signal line driving circuits for supplying a current to the level shifter based on the pulse from the shift register(see column 4, lines 15-20; 46-57).

While teaching the usage of a source line and gate line driving circuits there fails to be any disclosure of a first to x-th unit included in the driving circuits, as recited in **claims 10, 46, 82, 152, 166**, or the usage of a decoder, as recited in **claims 73, 82, 109, 118, 159**. Also, Kwon fails to specifically teach wherein only when said plurality of shift registers in said a-th unit serially outputs the pulses, said a-th current source supplies the current and said level shifters are operated.

Callahan et al. teaches a source signal line driving circuit (14) composed of signal drivers 1-11 and a gate line driver (16) composed of a plurality of fate drivers (see Figure 2). There is also taught the usage of a decoder (30) included in the source signal line driving circuit for outputting pulses n accordance with input signals (see column 5, lines 39-50).

Marshall et al. teaches a power regulator wherein a shift register, having a plurality of stages, or units (see column 2, lines 9-15), operates with respect to clock pulses from a clock signal in which the clock signals are generated in association with the power control pulses.

That is upon initiation of the power regulator a fist clock signal is output to the shift register, the shift register output terminals are set to a first level and the shift register will output a signal on successive occurrences of the second clocking signal (see column 5, line 16-column 6, line 15).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of a source and gate line driving circuit having a plurality of units and a decoder similar to that which is taught by Callahan et al. to be used in a display device similar to that which is taught by Kwon et al. wherein the current source only supplies current when the shift register is outputting pulses similar to that which is taught by Marshall et al. in order to thereby provide a display device which is capable of generating high quality images for a large display device without consuming a excess of power.

With reference to **claims 11, 47, 74, 83, 110, 119, 153, 160, and 167**, while not specifically teaching that the source and gate line driving circuits and the pixel portion are provided over a glass substrate, Kwon et al. does teach conventional active matrix displays including a plurality of transistors and capacitors on a glass substrate (see column 1, lines 32-35).

The examiner takes Official Notice in that it is well known, and obvious to one skilled in the art, for the source and gate line driving circuits and the pixel portion to be provided over a glass substrate.

Therefore it would have been obvious to one having ordinary skill in the art to allow for the source line driving circuit, the gate line driving circuit, and the pixel portion to be provided over a glass substrate as well known in the art and suggested by Kwon et al. in order to provide a transparent surface for constructing the display device for displaying images.

With reference to **claims 12, 13, 48, 49, 75, 76, 84, 85, 111, 112, 120, and 121**, neither Kwon et al. nor Marshall teaches that the driving circuit is provided on the same or different substrate as the pixel portion.

However, while not specifically teaching that the driving circuits and the pixels circuits are disposed on the same or different substrates, the Examiner takes Official notice in that conventional display devices are well known to have both of these configurations.

Therefore it would have been obvious to one having ordinary skill in the art to allow for the driving circuits and the pixels to be formed on the display substrates in accordance with what is conventionally known allowing placement on either one substrate or both of the substrates in order to produce a display device capable of display images.

With reference to **claims 14-18, 50-54, 77-81, 86-90, 113-117, 122-126, 154-158, 161-165, and 168-184**, while Kwon et al. teaches the usage of flat displays such as liquid crystal display (see column 1, lines 15-20) there fails to be any disclosure of the display device being incorporated into a personal computer, portable information terminal, car audio set, or digital camera.

However, the examiner takes Official Notice in that it is well known in the art for display device, preferably LCD device to be incorporated into personal computers, portable information terminals, car audio sets, and digital cameras.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of the LCD, similar to that which is taught by Kwon et al. in a wide range of user devices thereby providing the user with a clearer image of the displayed information.

With reference to **claims 174, 176-180, and 182-184**, while Kwon et al. teaches the usage of a source signal line driving circuit and a gate signal line driving circuit, wherein the source signal line driving circuit includes a latch type transmission array comprising thin film transistors (see column 5, line 45-column 6, line 12), there fails to be any other specific disclosure of the driving circuits comprising thin film transistors.

However, the examiner takes Official Notice in that it is well known in the art for the driving circuits of a display device to comprise of thin film transistors.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of thin film transistors in the driving circuits in order to thereby provide appropriate driving signals to drive the image onto the display device.

Response to Arguments

Applicant's arguments filed June 26, 2006 have been fully considered but they are not persuasive.

With respect to the drawing objection, as shown from above, it has been withdrawn. Applicant argues where the prior art of Kwon et al in combination with Marshall and Callahan fail to teach the limitations of a current source for supplying a current to a level shifter based on a pulse from the shift register or a decoder and that only when the shift register or decoder serially outputs pulses, the current source supplies the current and the level shifter is operated. Examiner, respectfully, disagrees. Kwon et al clearly teach a current source (46, 58) for supplying a current to the level shifter based on the pulse from the shift register(see column 4, lines 15-20; 46-57), but fails to teach wherein only when said shift register serially outputs the pulses, said current source supplies the current and said level shifter is operated.

Marshall et al. teaches a power regulator wherein a shift register, having a plurality of stages, or units (see column 2, lines 9-15), operates with respect to clock pulses from a clock signal in which the clock signals are generated in association with the power control pulses. That is upon initiation of the power regulator a fist clock signal is output to the shift register, the shift register output terminals are set to a first level and the shift register will output a signal on successive occurrences of the second clocking signal (see column 5, line 16-column 6, line 15).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of the shift register with multiple stages wherein power is only provided when the shift register output pulses as taught by Marshall et al. in a device similar to that which is taught by Kwon et al. in order to thereby provide a display device in order to improve power regulation for reducing power consumption of the display. Thus, the rejection is maintained and made FINAL.

Conclusion

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

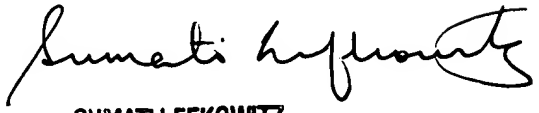
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srilakshmi K. Kumar whose telephone number is 571 272 7769. The examiner can normally be reached on 9:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571 272 3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Srilakshmi K. Kumar
Examiner
Art Unit 2629

SKK
September 29, 2006



SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER